

**CCRAFT SA**

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## Job ID: CAD2603

### **PIC Physical Design & Layout Engineer**

#### **The company**

CCRAFT is an independent photonic chip foundry specializing in thin-film lithium niobate (TFLN) technology. Built on over six years of development carried out entirely in an industrial manufacturing environment, CCRAFT now transitions to full-scale production. With in-house fabrication and a validated Process Design Kit (PDK), we address needs across telecom, datacom, quantum, and sensing markets. Our offering includes multi-project wafer (MPW) runs, custom dedicated fabrication, and scalable production. By uniting industrial manufacturing with design enablement, CCRAFT accelerates the deployment of next-generation photonic systems.

#### **The role**

We are seeking a **PIC Physical Design & Layout Engineer** to design, integrate, and prepare photonic integrated circuits for manufacturing on CCRAFT's TFLN platform. The role focuses on physical design, layout, and tapeout of customer and internal chips, ensuring compliance with PDK rules, fabrication constraints, and packaging and measurement requirements. You will translate system and component specifications into manufacturable chip layouts, perform DRC/LVS and design sign-off, and generate production-ready mask data and reticles.

You will work closely with component simulation, PDK, fabrication, and measurement teams to ensure that designs are physically correct, scalable, and aligned with the full production flow, from design to wafer-level integration and testing.

#### **Responsibilities**

##### **Physical Design & Layout**

- Design and implement full-chip layouts for PICs using CCRAFT's design kits.
- Perform floorplanning and hierarchical integration of complex PICs.
- Translate system, component, and customer specifications into manufacturable designs.
- Generate production-ready GDS and reticle data for fabrication.

##### **Verification & Tapeout**

- Run and debug DRC/LVS and other physical verification checks to ensure design compliance with foundry rules.
- Own tapeout quality and design sign-off for internal and customer chips.
- Identify and resolve layout-related issues impacting yield, performance, or reliability.
- Prepare and validate mask sets and reticles for MPW and dedicated production runs.

##### **Technology & PDK Integration**

- Apply PDK rules, layer definitions, and design constraints consistently across all designs.
- Contribute to PDK improvement by identifying missing rules, design bottlenecks, and layout limitations.

##### **Packaging, Test & Manufacturing Alignment**

- Integrate packaging and assembly constraints into chip layouts.
- Ensure chip designs include appropriate test and characterization structures.

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- Work closely with simulation, fabrication and measurement teams to correlate layout choices with process and test results.
- Support yield analysis and layout-driven process improvements.

## Requirements

### Essential

- MSc or PhD in Photonics, Electrical Engineering, Physics, or a closely related field.
- 3+ years of hands-on experience in PIC physical design and layout.
- Strong experience with DRC/LVS, tapeout, and design sign-off flows.
- Proficiency with PIC layout and mask design tools (e.g. IPKISS, GDSPy, GDSFactory, Cadence, L-Edit, or equivalent).
- Solid understanding of PDK structures, layer stacks, P-cells, and physical design rules.
- Good understanding of photonic component physics and simulation principles.
- Comfortable using Python or similar scripting tools for layout automation and data handling.
- Ability to operate in a fast-paced startup environment with high autonomy and responsibility.
- Excellent written and spoken English.

### Nice to have

- Hands-on experience with photonic component simulation.
- Familiarity with packaging and assembly constraints for PICs.
- Exposure to fabrication processes and yield-driven design improvements.
- Experience supporting PIC characterization.

## Conditions & Benefits

- Permanent position, competitive salary, performance bonus, ESOP participation.
- Based at CCRAFT's office in Western Switzerland, with flexible hybrid scheme.
- Collaborative, low-hierarchy team, valuing initiative, transparency, and growth.
- Being a core team member in a high-potential startup with global impact and recognition, shaping CCRAFT's design and integration ecosystem.
- Professional development through conferences, training, and industry engagement.

## How to apply

Send your application to [careers@ccraft.com](mailto:careers@ccraft.com) (email subject: **CAD2603\_YourName**) as a **single file CAD2603\_YourName.pdf** containing:

- 1-page cover letter outlining what you bring to CCRAFT, what CCRAFT brings to you, and what CCRAFT and you could bring to others.
- 2-page CV with focus on relevant experience.
- Contact details for 2 references.

**Application deadline: Feb 10<sup>th</sup> 2026.** We will evaluate applications as soon as they come in and contact you shortly after your submission.